SynTest-Magma

Integrated RTL-to-GDSII DFT Flow for ASICs

SYNTEST
The Testability Company

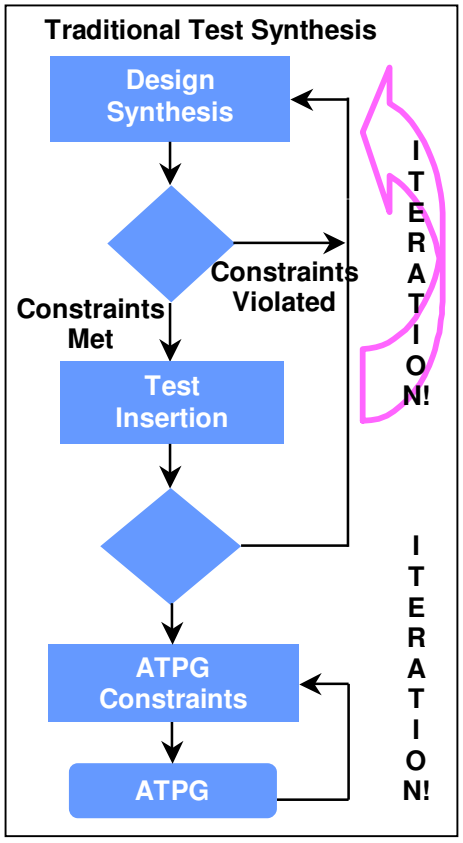
Design-for-Test (DFT) tools and methodologies enable automatic incorporation of many aspects of the semiconductor testing technologies, ensuring that the device comes through tape-out and manufacturing on time, according to specifications and of good quality. DFT tools enable creation of testable designs and efficient test patterns that detect most major manufacturing defects.

The most prevalent DFT methodology to attain high fault coverage comprises scan insertion and Automatic Test Pattern Generation (ATPG).

In the traditional test synthesis method, scan chains are inserted after logic synthesis. This results in an iterative process involving scan placement trials, to ensure that all constraints related to layout and timing closure are properly met. The end effect being that this could result in a significant delay to the overall product schedule.

BENEFITS

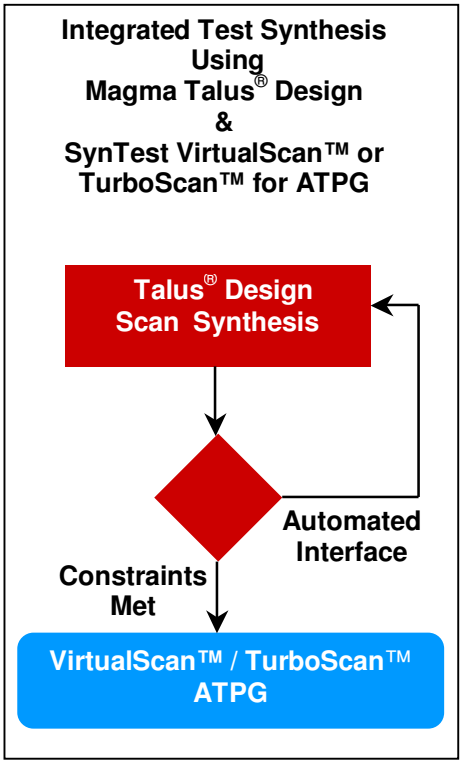
- **Improves quality and reduces time & costs for ASIC design and test.**
- **Automated, clean and portable design flow.**
- **Concurrent logic and scan synthesis in Talus® Design.**
- **Easy-to-use, single command interface to SynTest ATPG.**
- **Re-stitching of scan-chains based on placement information in .def file from Talus® Vortex.**
- **Rapid, efficient test vectors from – VirtualScan or TurboScan.**



Focusing on successful DFT implementation without unnecessary iterations, SynTest and Magma have partnered to provide a seamless interface that ensures that layout and timing constraints are met with a single tool flow.

The Magma's design environment, Talus®, includes a built-in, full-featured one pass scan insertion and optimization engine.

It provides an easy, single-command interface to SynTest VirtualScan™ or TurboScan™ ATPG by accepting STIL as input.



VirtualScan provides XtremeCompact test vectors that significantly reduce the costs and time on the ATE.

Integrated DFT and Synthesis Solution for ASICs

SynTest **DFT-PRO Plus™**, a DFT tool suite, tightly couples with Magma's design, synthesis and layout products to provide engineers with a complete 'RTL to GDSII' solution and an effective product design and test flow.

DFT-PRO *Plus*™ offers an integrated DFT solution covering scan synthesis and ATPG, memory BIST synthesis and boundary-scan (JTAG) synthesis. The corresponding tools generate RTL blocks that fit seamlessly into an existing synthesis flow.

BENEFITS

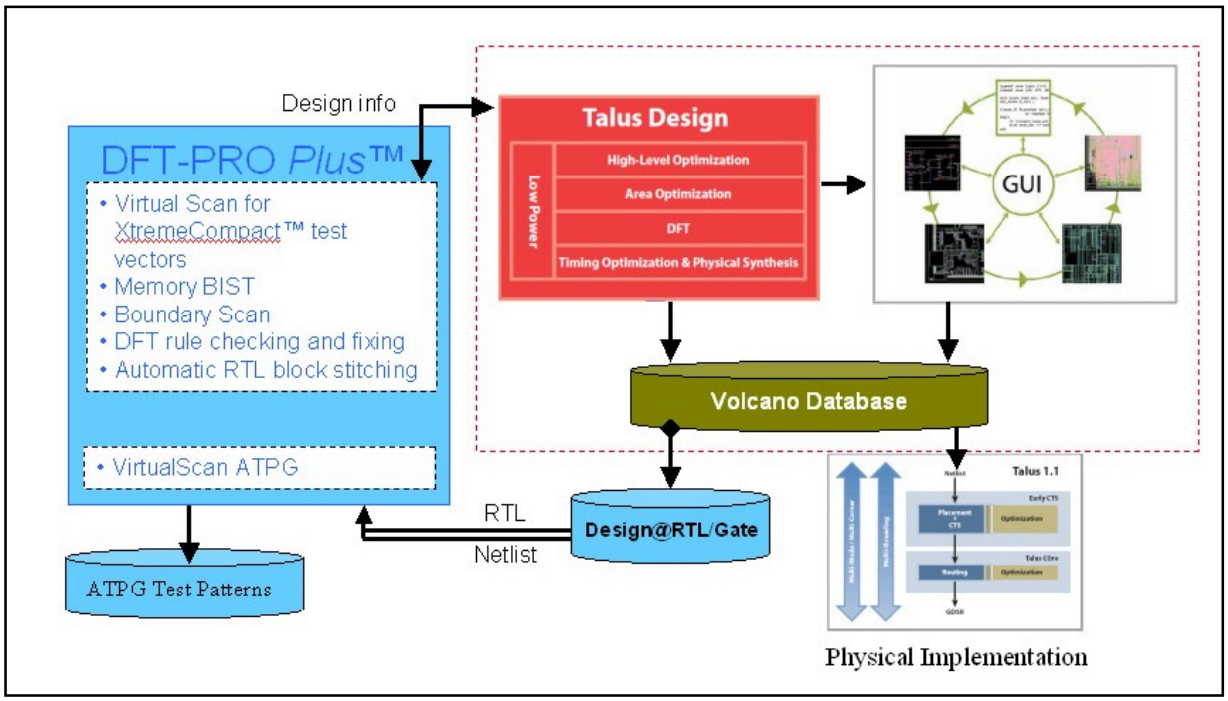
- **Improves quality and reduces time & costs for ASIC design and test.**
- **Allows a quick "what-if" analysis on DFT structures at the RTL and their impact on overall area, timing, power, etc.**
- **Checks DFT rule violations at the RTL to avoid expensive iterations.**
- **Integrates Magma Talus® Design environment with SynTest DFT-PRO Plus™, which includes VirtualScan™, to reduce ATE and test costs.**

The block diagram alongside shows the integrated DFT and synthesis solution for ASICs that enables Magma users who use the Talus® Design environment for logic synthesis, in conjunction with Magma Talus® Vortex Placement and Routing environment, to perform automatic insertion of scan chains, followed by compact, high fault coverage ATPG, in one pass.

The diagram depicts a comprehensive flow for insertion of DFT technology into a typical ASIC design, covering scan/ATPG, memory BIST and boundary-scan synthesis, as well as checking for DFT rule violations at both RTL and gate-level stages of an ASIC design.

The DFT tools generate DFT blocks at the RTL that fit seamlessly into an existing synthesis flow and also ease the design floor planning process.

Further checking DFT violations at the gate level averts costly and time-consuming post-synthesis surprises.



Application:
RTL testability rule check

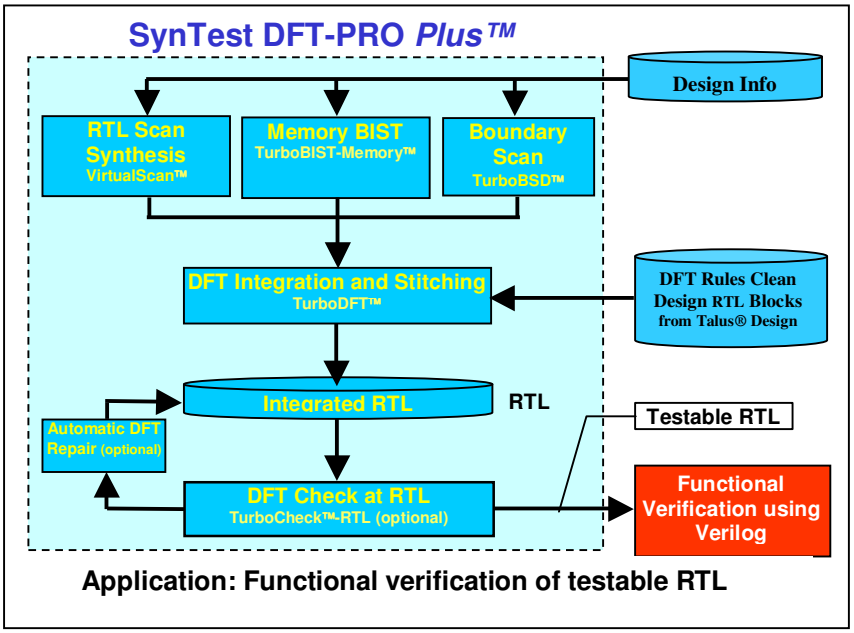
Magma Interface: Talus® Design

SynTest Interface: TurboCheck-RTL

Magma Talus® Design has capability of comprehensive DFT rules violations checking before the design is fed to SynTest DFT tools.

The DFT blocks generated at the RTL by various SynTest DFT tools and the design RTL blocks are automatically stitched together by SynTest TurboDFT to generate a whole RTL circuit.

Before being fed as a testable RTL, via a Magma Talus® Design platform interface for functional verification, the integrated RTL is fed to SynTest TurboCheck-RTL to check for DFT rule violations.



Application: Functional verification of testable RTL

Designers can very quickly identify testability problems at the earliest stages of the design cycle, even before the often time-consuming logic synthesis process. TurboCheck-RTL can also be used to identify adherence to design guidelines and synthesis constraint violations. TurboCheck tools find key testability problems quickly and automatically, including floating nets, busses and ports, combinational feedback loops, uncontrollable or unobservable nodes, potential bus contention, gated clocks, sequentially generated clocks, and asynchronous set/reset conditions.

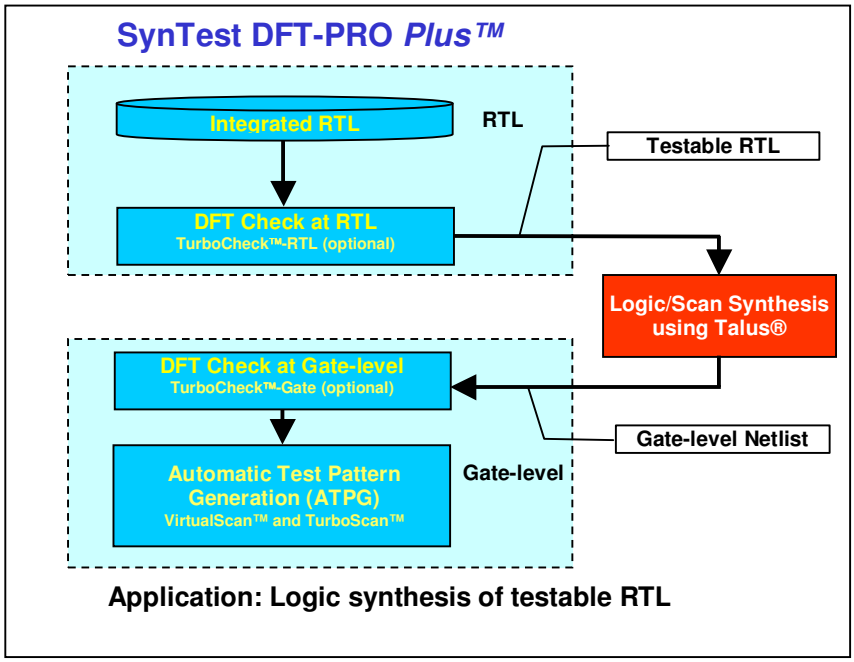
Application:
Logic synthesis of testable RTL

Magma Interface: Talus® Design

SynTest Interface: TurboCheck-Gate and TurboScan

The testable RTL is fed to Talus® Design for logic synthesis. Talus® Design generates a gate-level netlist that is used for scan synthesis and ATPG. Outputs from Talus® Design are also fed to Magma Vortex for placement and routing.

Designers can perform a structural level check on the final synthesized design, using TurboCheck-Gate, to further identify and zero-in on any gate-level testability violations that could not be detected at the RTL.



Application: Logic synthesis of testable RTL

TurboCheck tools find many testability problems quickly and automatically, including floating nets, busses and ports, combinational feedback loops, uncontrollable or unobservable nodes, potential bus contention, combinationally gated clocks, and sequentially generated/gated clocks and asynchronous set/reset condition. TurboScan-ATPG also offers automatic insertion of test points using a selection algorithm and analyzes the effect of the selection on the testability of the circuit.

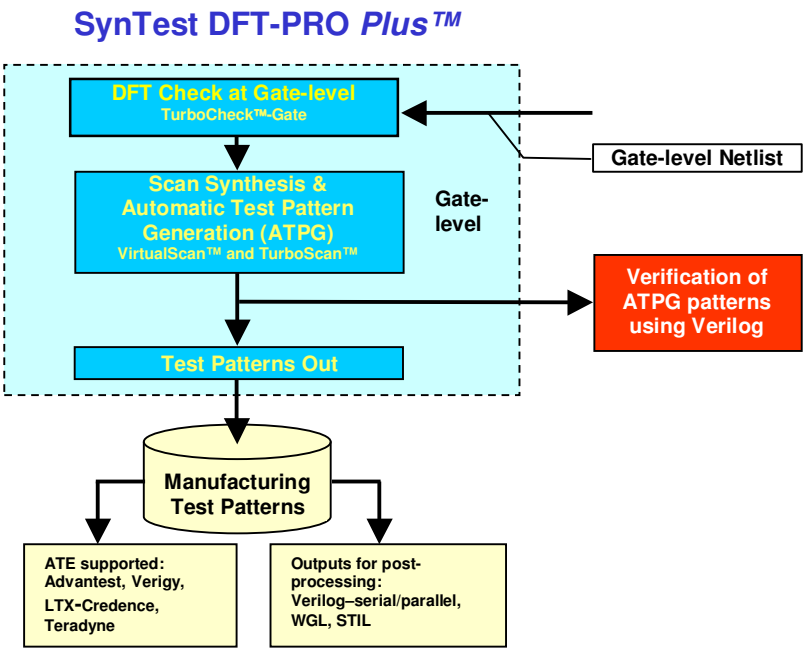
Application:
Generation of compressed scan patterns and ATE test programs

Magma Interface: Talus® Design

SynTest Interface: VirtualScan

VirtualScan™ is a tool for scan insertion and ATPG with test compression capability to generate XtremeCompact scan test patterns. This reduces the scan test cost by a factor of 5x to 100x through reduced test data volume, test application time and ATE reloads.

These ATPG patterns are fed via TP-out, as testbenches and manufacturing test patterns, and are available in a variety of ATE formats, including Advantest, LTX-Credence, Teradyne, and Verigy.



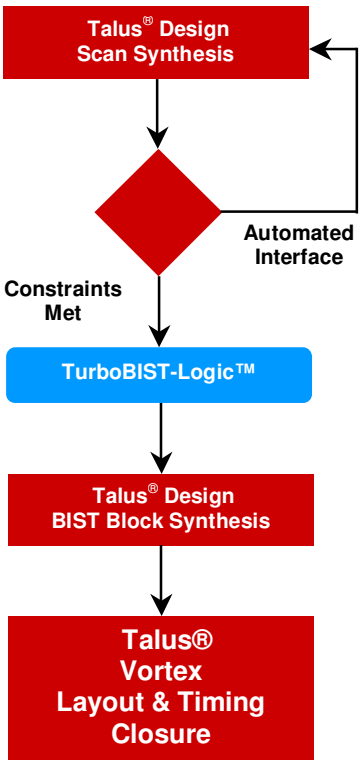
Application: Functional verification of ATPG patterns

Application:
Physical synthesis and integration of Logic BIST blocks

Magma Interface: Talus® Vortex

SynTest Interface: TurboBIST-Logic

Talus® Design provides a gate-level netlist. Based on it, TurboBIST-Logic generates logic BIST blocks consisting of a central BIST controller and needed Pseudo-Random Pattern Generators (PRPGs) and Multiple-Input Signature Registers (MISRs). These are fed to Talus® Design for BIST block synthesis, and subsequently to Talus® Vortex for placement and routing. The BIST blocks can also be inserted at the RTL during pre-synthesis.



Application: Physical synthesis and integration of Logic-BIST blocks

SynTest Technologies, Inc.
505 S. Pastoria Ave, Suite 101, Sunnyvale, CA 94086
Tel: 408-720-9956 Fax: 408-720-9960

www.syntest.com
info@syntest.com